ADQ32 Datasheet

The ADQ32 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ32 features:

- **One analog channel at 5 GSPS included**
- **Two analog channels at 2.5 GSPS per channel included**
- **Sampling rate option at 4 GSPS and 2 GSPS respectively**
- **12 bits resolution**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**

1 ORDERING INFORMATION

ADQ32 is available with a set of options. Follow the procedure to configure the ADQ32. Start with the hardware configurations. These are factory installed and cannot be changed through software commands.

1. Select clock rate option **-S2G5** (standard) or **-S2G0** (optional).
2. Select the DC-coupled analog front-end **-DC** (standard). For dual-gain **-PDRX** analog front-end, see 22-2797 ADQ32-PDRX datasheet.
3. Select the analog bandwidth **-BW1G0** (standard) or **-BW2G5** (optional)

Select the firmware options. The firmware FWDAQ is always included. Additional firmware files are distributed as files and can be loaded into the board at any time.

4. Data acquisition firmware **-FWDAQ** is always included
5. Select one or several of available firmware packages, **-FWATD**, **-FWPD**.
6. Select to activate channel combination option for dual-gain pulse detection, **-LICPDRX**[1].
7. Select accessories, open FPGA development kit **DEVDAQ**, **-DEVPD**[2].
8. Select extended warranty **-W5Y**.

The open FPGA is accessed through the design project for each firmware. For **-FWDAQ**, the development kit is **DEVDAQ**. For **-FWPD**, the development kit is **DEVPD**. The **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project can be used on any ADQ32 with a valid FWDAQ license (included on all units).

[1] See 22-2797 ADQ32-PDRX datasheet for more information about dual-gain channel combination. The ADQ32 can be used with external dual-gain amplifier and channel combination in firmware. The option LICPDRX activates the channel combination for external dual-gain amplifier.
[2] DEVPD is available in 2024. Contact Teledyne SP Devices for more information.

Table 1 Valid combinations of options

Options	DC-S2G0	DC-S2G5 [3]	Comment
Hardware options			
BW1G0 [3]	✓	✓	Standard
BW2G5		✓	Optional
PCIe	✓	✓	Standard
Firmware options			
FWDAQ	✓	✓	Always included
FWATD	✓	✓	Optional
FWPD	✓	✓	Optional
LICPDRX [4]	✓	✓	Optional
Additional accessories			
DAQDEV	✓	✓	Separate item
DAQPD	✓	✓	Separate item
W5Y	✓	✓	Extended warranty [5]

[3] Standard version. If a parameter is not specified, the standard version is delivered.
[4] See ADQ32-PDRX datasheet 22-2797 for more information about dual-gain channel combination.
[5] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices. Warranty extension must be ordered before included 3 years warranty is expired.

2 ADQ32 INTRODUCTION

2.1 Features

- One and two analog input channels
- 5 and 2.5 GSPS sampling rate per channel
- 12 bits resolution
- DC-coupled with 1 GHz bandwidth (optional 2.5 GHz)
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD
- Pulse analysis firmware FWPD

2.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight mass spectrometry
- Distributed Optical Fiber Sensing
- LIDAR
- Scientific instruments
- Scanning acoustic microscopy

2.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ32 offers a variety of options for efficient system design:

Streaming to GPU
ADQ32 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ32 supports up to 7 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ32 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

Pulse data recording
The hardware option ADQ32-PDRX offers a built-in dual-gain amplifier for pulse data capture with extended dynamic range. See datasheet 22-2797 for more details on the option ADQ32-PDRX.

3 TECHNICAL DATA

Technical parameters are valid for ADQ32 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 2 Analog input (front panel label A and B) standard bandwidth 1 GHz

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels	2 channels mode		2		
Sampling rate per channel	2 channels mode	See table Table 4			
Number of channels	1 channel mode		1		
Sampling rate	1 channel mode	See table Table 4			
Bandwidth -3dB	Standard config.		1		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type		SMA			
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode					
Cross talk	< 1 GHz		-70		dBFS
Noise power density	0 to 1.25 GHz		-148		dBFS/√Hz
SNR	260 MHz, -1dBFS		55		dBc
SFDR	260 MHz, -1dBFS		66		dBc
ENOB relative full scale	10 MHz, -1dBFS		9		bits
ENOB relative full scale	260 MHz, -1dBFS		8.9		bits
ENOB relative full scale	810 MHz, -1dBFS		8.5		bits
Dynamic performance, 1 channels mode, no FIR filter, connector A[6]					
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		65		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.9		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	810 MHz, -1dBFS		8.5		bits
Dynamic performance, 1 channels mode, FIR filter[7], connector A[6]					
SNR	260 MHz, -1dBFS		57		dBc
ENOB relative full scale	10 MHz, -1dBFS		9.2		bits
ENOB relative full scale	260 MHz, -1dBFS		9.2		bits
ENOB relative full scale	810 MHz, -1dBFS		9.1		bits

[6] Performance parameters are valid for 1 channel mode using input A. There are no parameters available for 1 channel mode using input connector B.

[7] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

Table 3 Analog input (front panel A and B) bandwidth option -BW2G5[8]

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels	2 channels mode		2		
Sampling rate per channel	2 channels mode	See table Table 4			
Number of channels	1 channel mode		1		
Sampling rate	1 channel mode	See table Table 4			
Bandwidth -3dB	Option **-BW2G5**		2.5		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode, option -BW2G5					
Cross talk	< 1 GHz		-70		dBFS
Noise power density	0 to 1.25 GHz		-147		dBFS/√Hz
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		63		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.8		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	810 MHz, -1dBFS		8.6		bits
Dynamic performance, 2 channels mode, FIR filter[9], option -BW2G5					
ENOB relative full scale	260 MHz, -1dBFS	bits	9.2		bits
Dynamic performance, 1 channel mode, no FIR filter, option -BW2G5, connector A[10]					
Noise power density	0 to 2.5 GHz		-150		dBFS/√Hz
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		65		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.8		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	1625MHz,-1dBFS		8.3		bits
Dynamic performance, 1 channel mode, FIR filter, option -BW2G5, connector A[10]					
ENOB relative full scale	810 MHz, -1dBFS		9.1		bits

[8] The analog bandwidth option -BW2G5 is factory installed and cannot be altered via software.

[9] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

[10] Performance parameters are valid for 1 channel mode using input A. There are no parameters available for 1 channel mode using input connector B.

Table 4 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator -S2G5 (standard) [11]					
Frequency range 1	2 channels	2440	2500	2500[12]	MHz
Frequency range 2	2 channels	1840		1970	MHz
Frequency range 1	1 channel	4880	5000	5000	MHz
Frequency range 2	1 channel	3680		3940	MHz
Internal sampling clock generator option -S2G0 [11]					
Frequency range 1	2 channels	1930	2000	2075	MHz
Frequency range 2	2 channels	1460		1540	MHz
Frequency range 1	1 channel	3860	4000	4150	MHz
Frequency range 2	1 channel	2920		3080	MHz
External clock reference input (from front panel CLK connector)[13]					
Frequency		1	10	500	MHz
Frequency [14]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [15]	AC		200		Ω
Clock reference output (on front panel CLK connector)[16]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω

[11] The internal clock generator can generate frequencies in 2 different ranges.
[12] The software setting limit. The tolerance with external clock reference is up to 2505 MHz.
[13] Using a clock reference from an external source to synchronize the ADQ32 to the external source.
[14] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[15] Software-selectable high-impedance mode.
[16] The internal clock reference of the ADQ32 is made available to synchronize external equipment.

Parameter	Condition	Min	Typical	Max	Unit
External direct sampling clock input (from front panel CLK connector)[17]					
Frequency [18]		1000		2505	MHz
Signal level		0.5		3.3	Vpp
Impedance	AC		50		Ω
Impedance	DC		10k		Ω
Physical connector label CLK					
Connector type		SMA			

[17] Using an external clock while bypassing the internal clock generator.

[18] In single-channel mode, the sampling frequency is 2 times the external clock frequency.

Table 5 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [19]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [20]	As trigger		50		ps
Update rate [20]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 6 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [19]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [20]	As trigger		3.2		ns
Update rate [20]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[19] Software-selectable high-impedance mode.

[20] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 7 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [19]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [20]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [20]				156.25	MHz

Table 8 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [21]	FWDAQ		30		W
Power supply		10.8	12	13.2	V
Operating temperature	FWDAQ[22]	0		55	°C
Operating temperature	FW options[23]	0		45	°C
Size					
Width			1		slot
Length			225.7		mm
Height			111.2		mm
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[21] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

[22] Operating the ADQ32 with FWDAQ and streaming data up to 7 GBPS.

[23] Using firmware options from Teledyne SP Devices. Custom firmware designs may result in higher power consumption and thereby lower temperature range.

Table 9 Custom GPIO expansion. See section 11.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

Table 10 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Rearm time[24]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2 channels mode in steps of 1	2		2^{32}-1	samples
	1 channel mode in steps of 1	2		2^{32}-1	samples
Pretrigger[25]	2 channels mode in steps of 8	0		16 360	samples
	1 channel mode in steps of 16	0		16 336	samples
Trigger delay[26]	2 channels mode in steps of 8	0		2^{35}-8	samples
	1 channel mode in steps of 16	0		2^{36}-16	samples

Table 11 Data transfer

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[27]	1 / 4 / 8	
Data rate to CPU sustained with headers	5	GByte/s
Data rate to CPU sustained without headers	7	GByte/s
Data rate to GPU sustained without headers	7	GByte/s
Data rate peer-to-peer to GPU sustained without headers	7	GByte/s

Table 12 Software support

Parameter	Value
Operating system[28]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[24] Minimum time from the last sample of a record to the next trigger.
[25] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[26] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[27] The ADQ32 must be installed in a 16 lanes slot or a slot with a connector with an open end.
[28] See 15-1494 Operating system support for a detailed listing of supported distributions.

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ32 features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

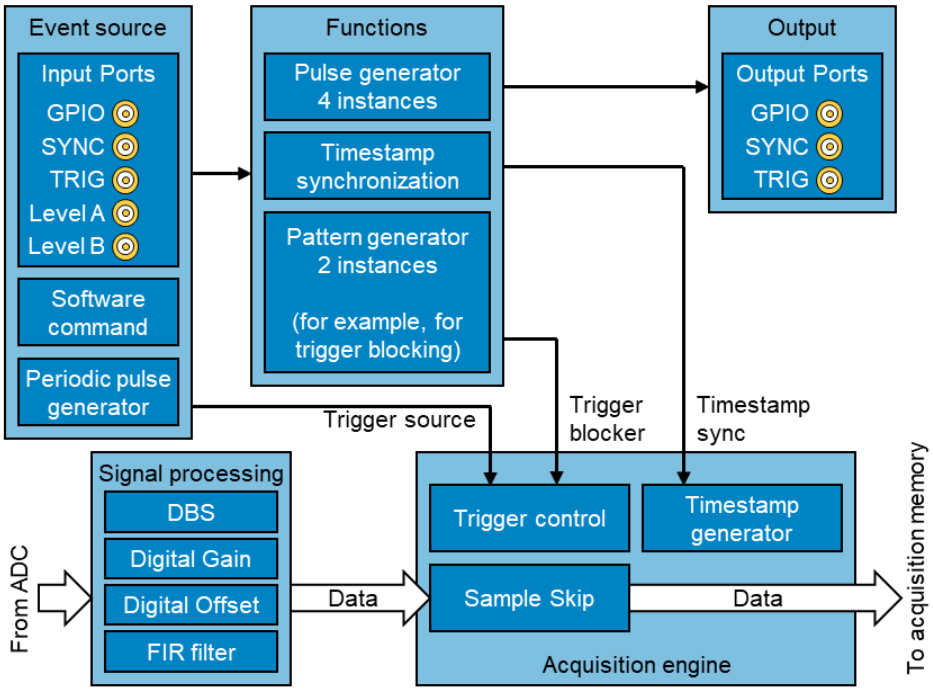


Figure 1 Flow control and synchronization block diagram.

Table 13 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 14 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ32.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ32.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 15 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp synchronization Control the time of the ADQ32.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 16 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli / control
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected **Trigger**
Data transfer modes Transport to CPU / GPU	Streaming with header Streaming without header	User set-up

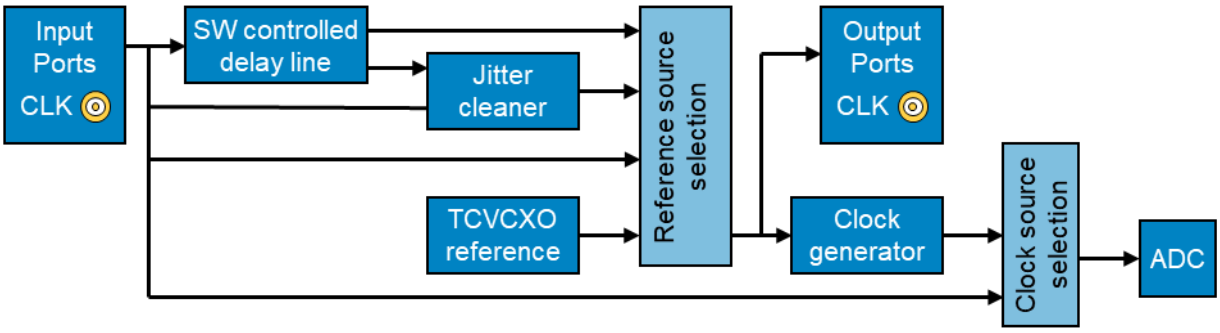


Figure 2 Clock generation block diagram.

Table 17 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The dual-gain channel combination included in FWDAQ requires a separate license for ADQ32.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The dual-gain channel combination included in FWATD requires a separate license for ADQ32.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The dual-gain channel combination is included in FWPD requires a separate license for ADQ32.

5.4 Managing firmware

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.
- Switching mode between one channel at 5 GSPS and two channels at 2.5 GSPS requires switching the digitizer firmware image.

6 ABSLOUTE MAXIMUM RATINGS

Table 18 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature [29]		0	55	°C
Analog in to GND		-1.75	+1.75	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V
FFC / FPC differential signal to GND	Powered[30]	-0.5	2.3	V
	Not powered[30]	-0.5	0.5	V
FFC / FPC single-ended signal to GND [30]	Powered[30]	-0.3	3.8	V
	Not powered[30]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[29] The absolute maximum temperature is the range where it is allowed to start the board.
The ADQ32 has a built-in overheat protection to prevent damage from overheat. The ADQ35 may therefore shut down at lower temperature than the absolute maximum.
The overheat conditions is depending on the load of the FPGA. For Teledyne SP Devices provided firmware options, see recommended operating conditions in Table 8. For custom firmware the temperature range has to be evaluated from case to case.
[30] The absolute maximum ratings depend on whether the ADQ32 is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

7.1 Frequency response

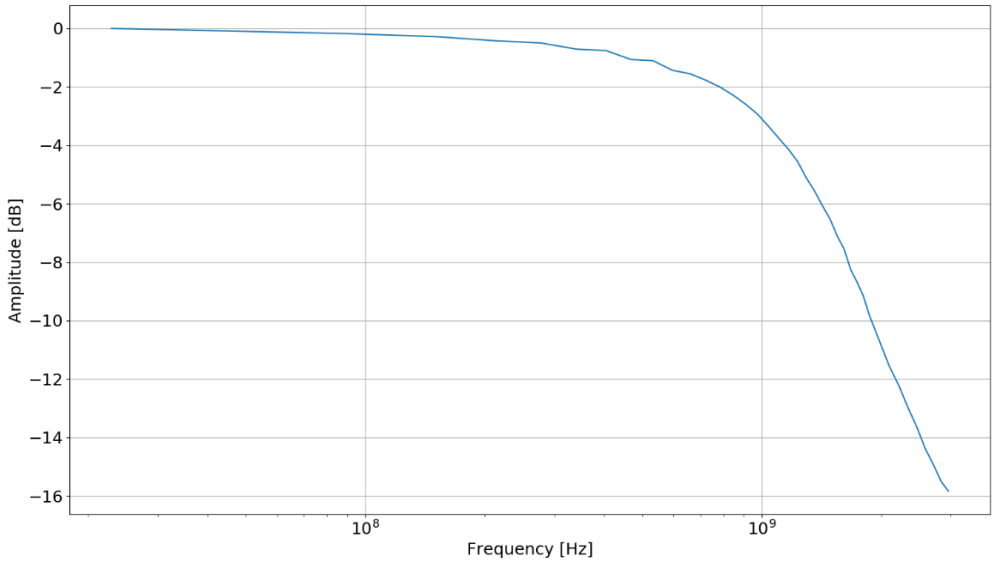


Figure 3 Frequency response, typical performance BW1G0.

7.2 FFT

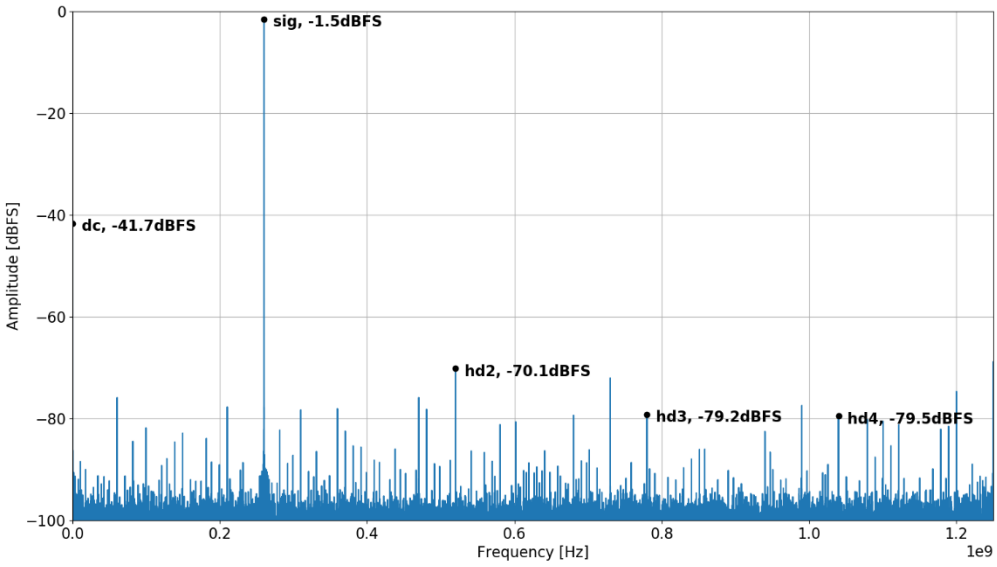


Figure 4 FFT typical performance 2.5 GSPS BW1G0.

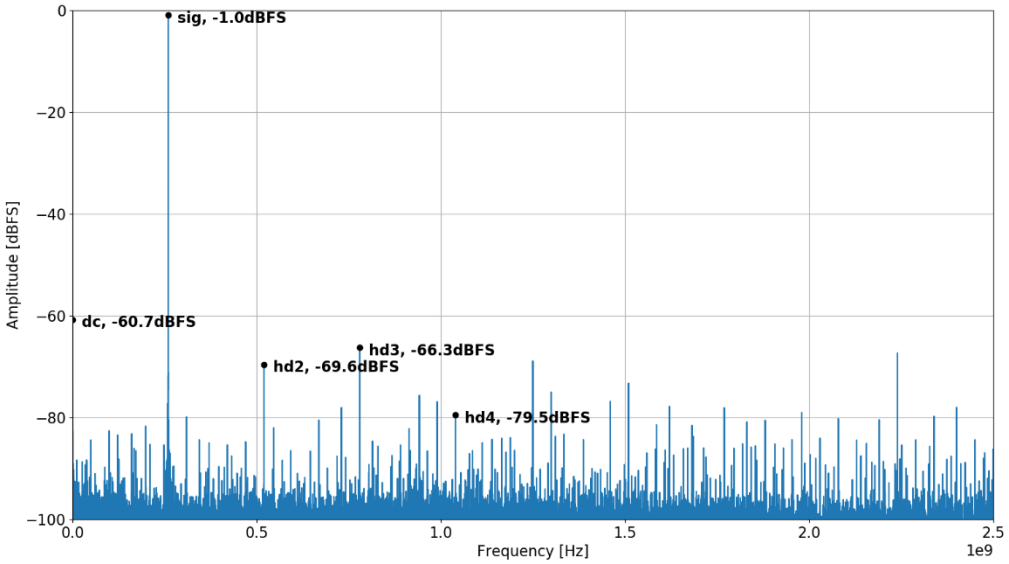


Figure 5 FFT typical performance at 5 GSPS, BW1G0

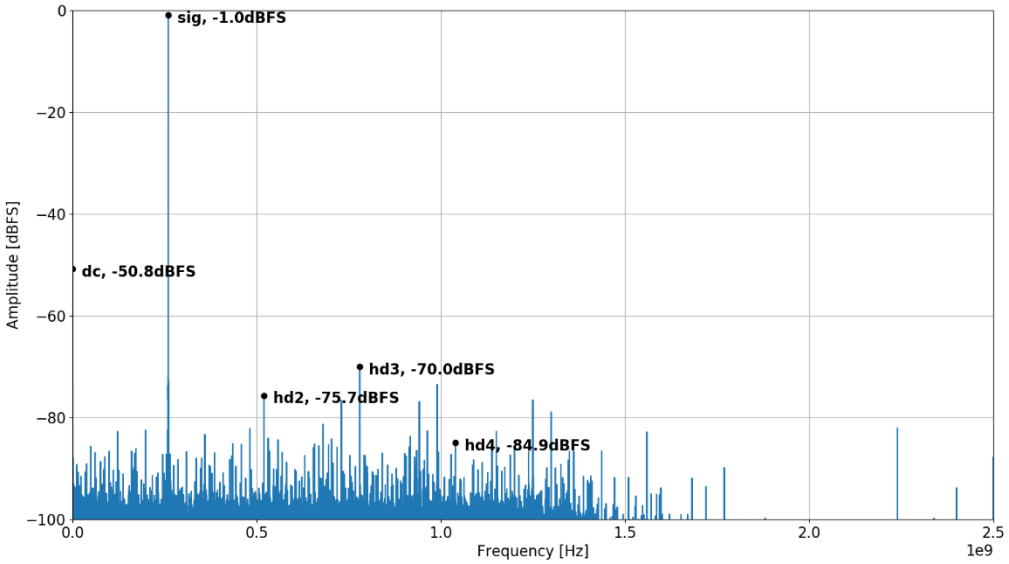


Figure 6 FFT typical performance 5 GSPS, using digital FIR filter, BW1G0.

8 TYPICAL PERFORMANCE BANDWIDTH OPTION -BW2G5

8.1 Frequency response

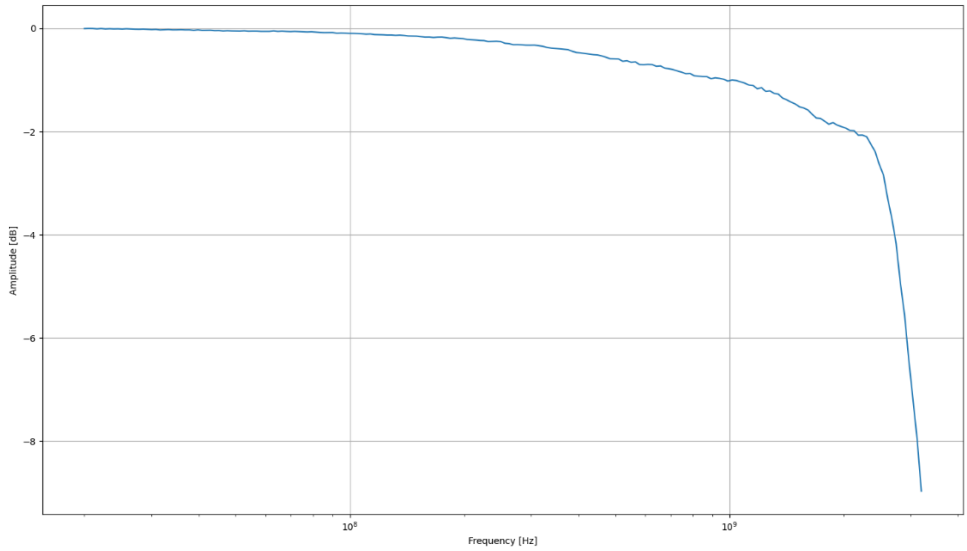


Figure 7 Frequency response, analog bandwidth option -BW2G5.

8.2 FFT

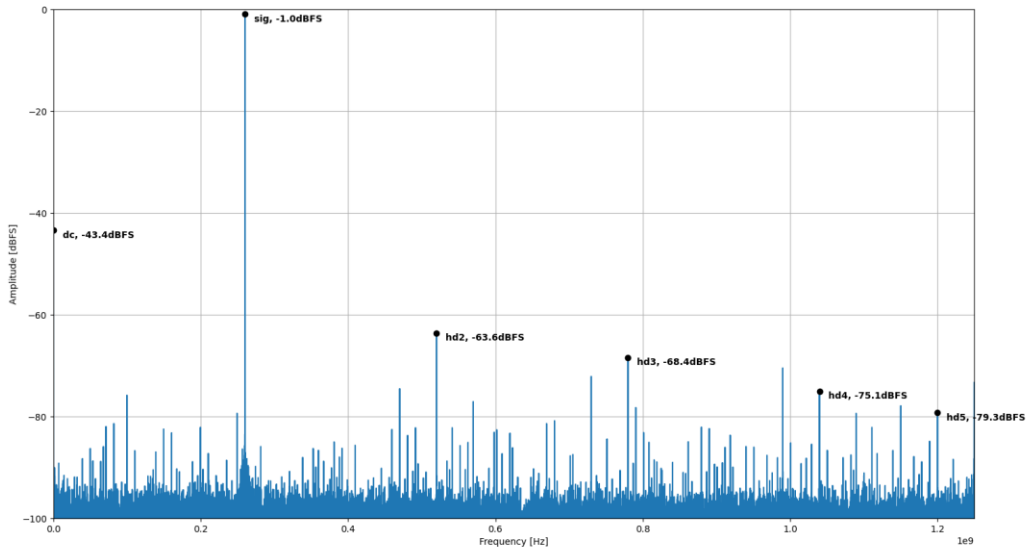


Figure 8 FFT typical performance 2.5 GSPS, analog bandwidth option -BW2G5.

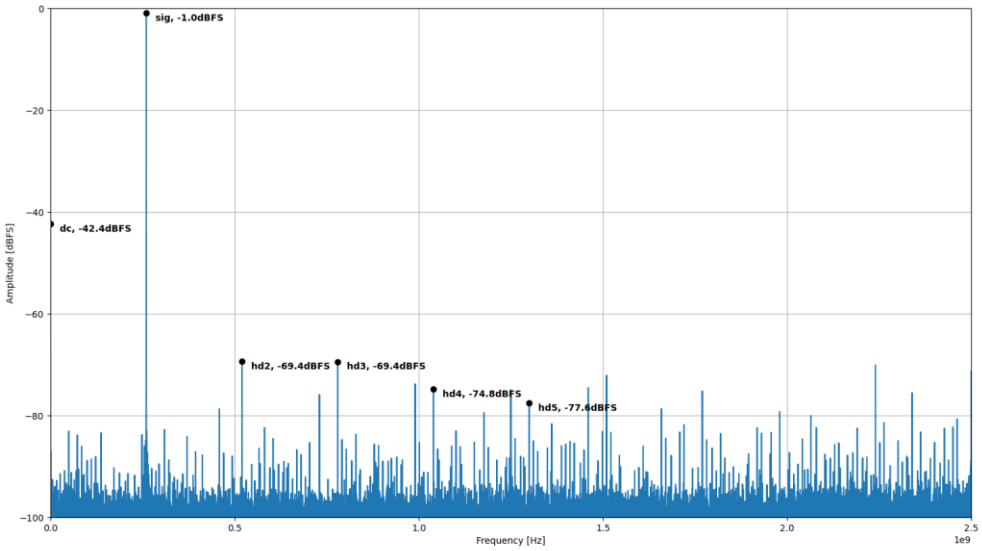


Figure 9 FFT typical performance at 5 GSPS, analog bandwidth option -BW2G5

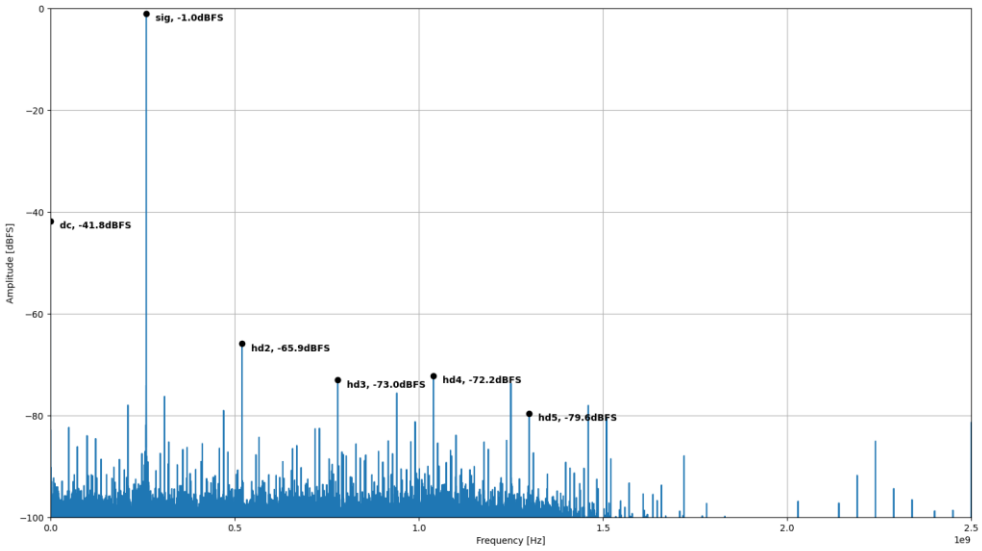


Figure 10 FFT typical performance 5 GSPS, using digital FIR filter, analog bandwidth option -BW2G5

9 BLOCK DIAGRAM

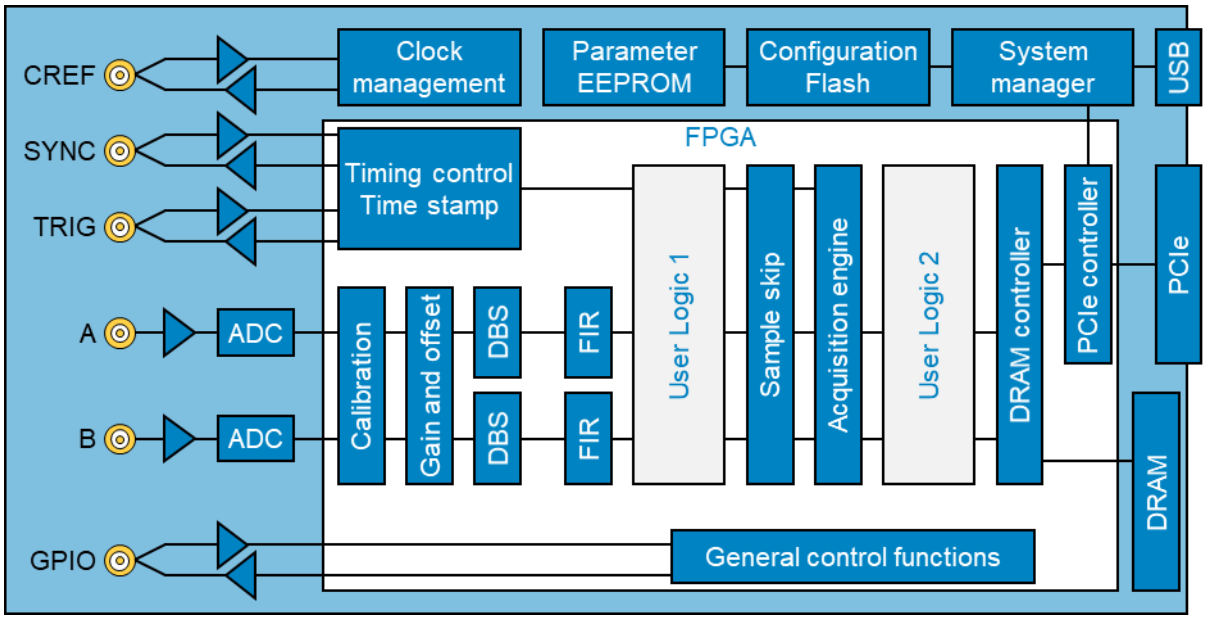
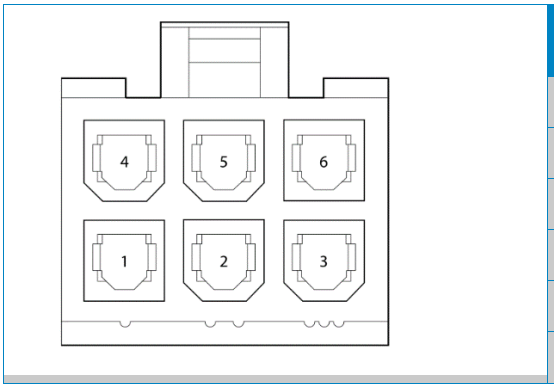


Figure 11 Block diagram.

Figure 11 shows a block diagram of ADQ32 in 2channels mode. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

10 HOST PC INTERFACE PCIE

The ADQ32-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 12. A suitable connector is for example Molex 45559-0002. It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 12 Power supply connection. Cable connector, looking into the connector end.

11 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ32 user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

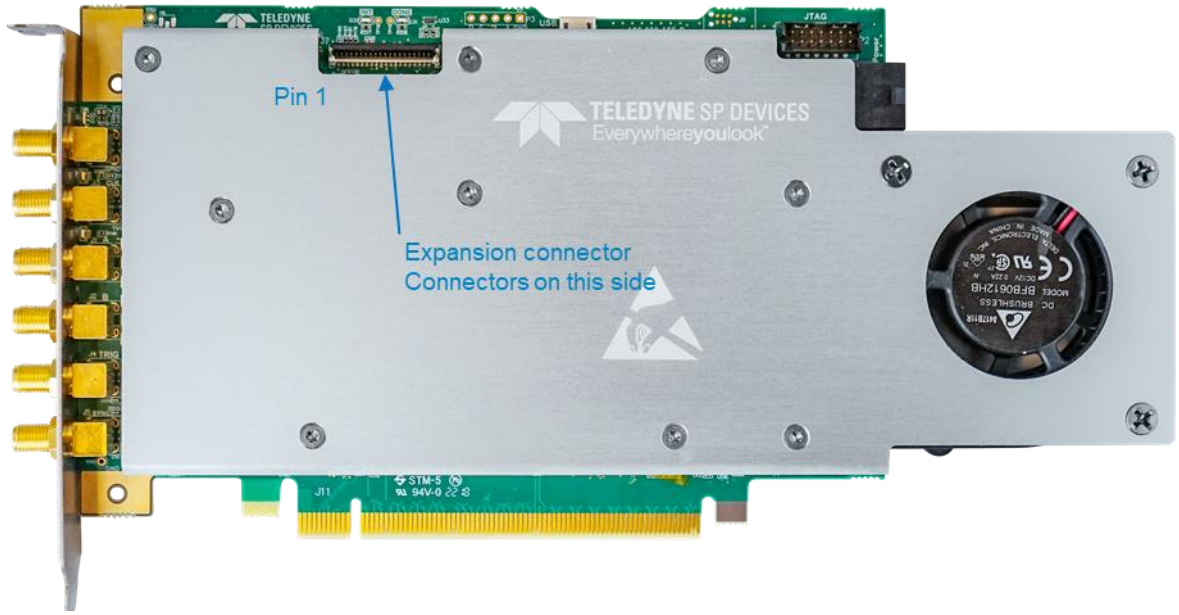


Figure 13 ADQ32 photo showing GPIO expansion connection on the top side.

12 MECHANICAL DRAWING

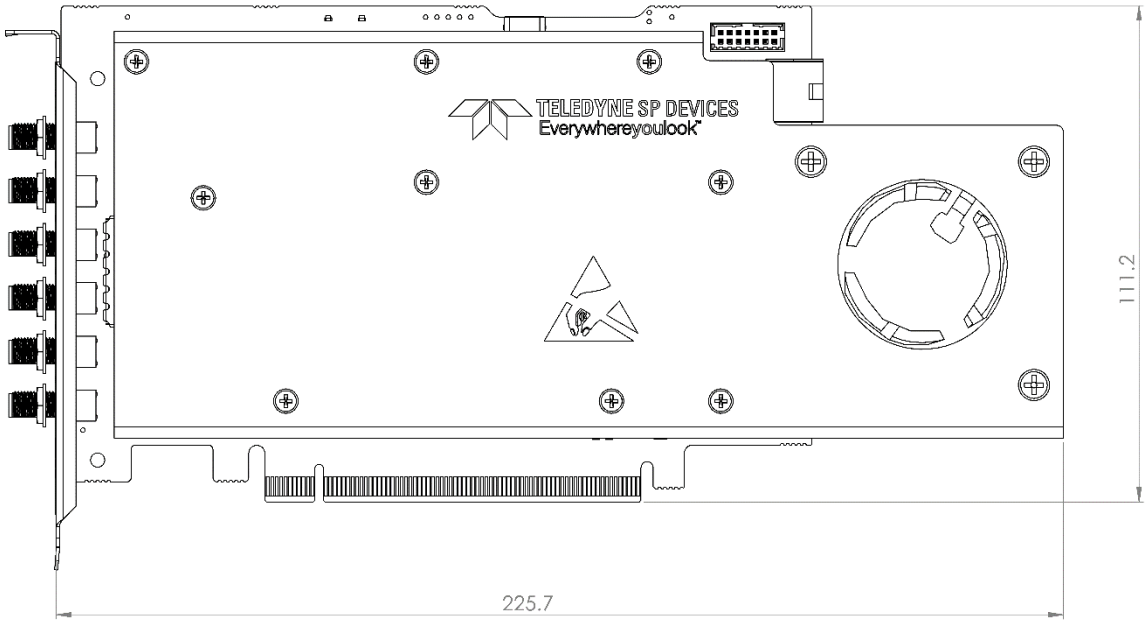


Figure 14 Mechanical drawing.

13 REFERENCES

Refer to TSPD's web site spdevices.com for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2797 ADQ32-PDRX datasheet

22-2912 ADQ3 FWATD datasheet

23-3028 ADQ3 FWPD datasheet

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www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 8D
SE-583 30 Linköping
Sweden
Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com